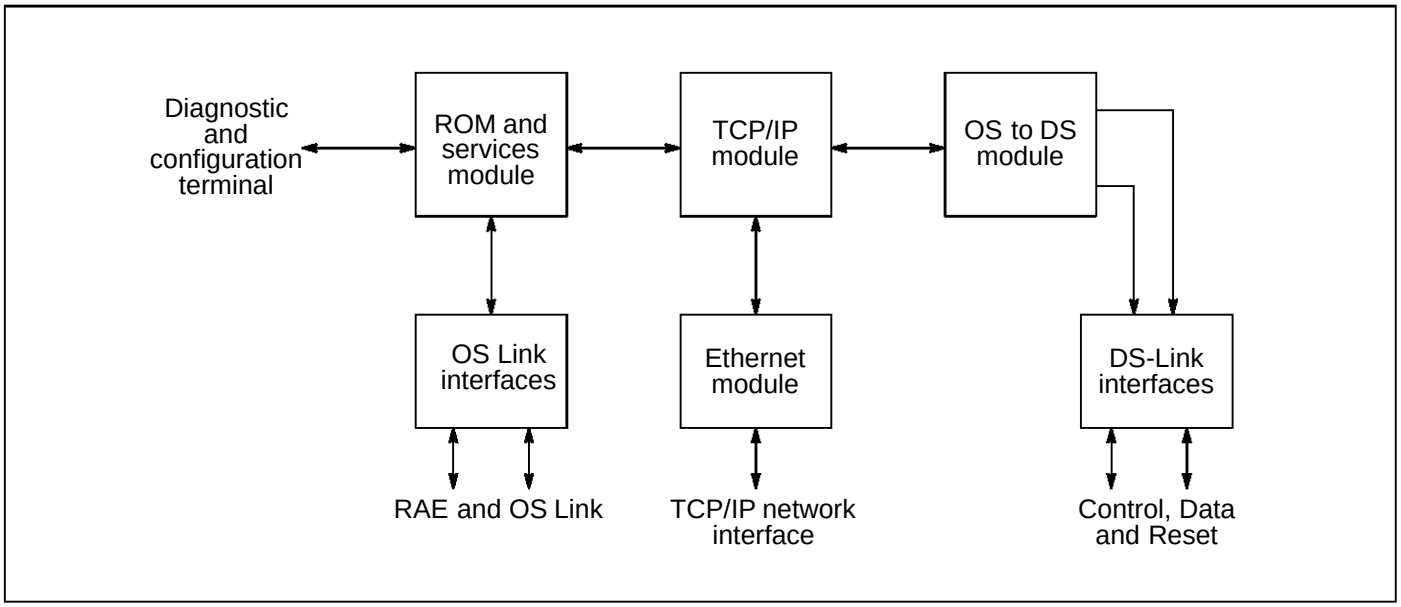
SGS-THOMSON MICROELECTRONICS

IMS B103

ETHERNET TO DS–LINK INTERFACE



FEATURES

- Single slot VME format system interface board
- Gateway between TCP/IP communications and DS link interface
- High performance TCP/IP protocol implementations in ROM
- Boot time loading of DS-Link interface and control code for easy maintenance and upgrade
- RS232 configuration and diagnostic port
- Single ended OS and DS subsystems on VME P2
- Differential OS and DS subsystem connections on front panel

DESCRIPTION

The IMS B103 is an interface gateway for communication between DS-Link based IMS T9000 systems and TCP/IP development environments. A high performance ROM based TCP/IP implementation allows boot time loading of interface software or applications onto an IMS T805 based interface circuit. Four ST C101 devices provide DS-Link control and data interfaces through both backplane and front panel connectors. The IMS B103 is compatible with both INMOS OS-Link and DS-Link based system interface standards.

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1.1 IMS B103 specification

The IMS B103 design is based on the IMS B300 and its related products [4]. A high performance multiprocessor implementation of the TCP/IP protocol stacks provides gateway support for both OS-Link and DS-Link based applications and development environments. An IMS T805/STC101 combination provides a high performance interface gateway between the TCP/IP environment and one or two T9000 networks.

The IMS B103 architecture is divided into two logical blocks:

- A TCP/IP interface block that comprises a system services module (ROM, RS232 interface and NVRAM), an ethernet interface module and a main IMS T805 transputer on which the TCP/IP protocol stack is actually run. This whole block is bootstrapped from ROM on the services module.
- An OS-Link to DS-Link conversion block based around an IMS T805 transputer and four STC101 DS-Link peripheral devices. This block can be bootstrapped with code from a network server or external development system.

The two blocks are connected together in a flexible manner (via a link jumper block) which allows a number of different configurations to be adopted. A block diagram of the board is shown in figure 1.1.

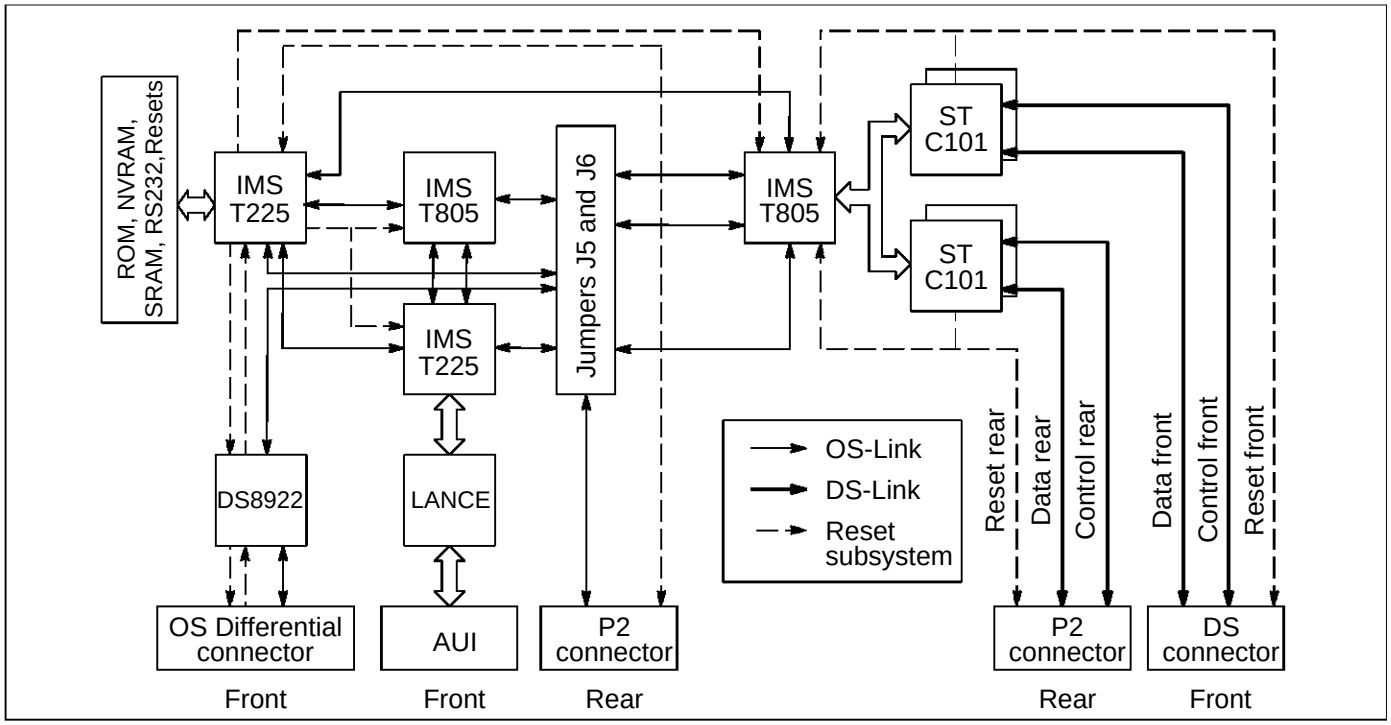

Figure 1.1 IMS B103 block diagram

The IMS B103 is supplied pre-programmed with the IMS F103 firmware to support a role as an interface for a T9000 development system. Other configurations and operational roles are possible, but these may involve additional firmware and/or software development.

1.2 Subsystems on the IMS B103

The IMS B103 has four separate reset subsystem regimes under control of the ‘Services’ IMS T225 module. These are connected to:

- The Ethernet module and TCP/IP module
- The OS to DS conversion module
- Front panel subsystem outputs
- Back panel subsystem outputs

The subsytem regimes connected to the OS to DS module and the front and back panel 5connectors can be manipulated by software running on the OS to DS subsytem. The principle use of this facility is to provide a route for application software running on the OS to DS module to control external hardware systems. Other facilities within the same interface allow OS to DS module applications to manipulate the front panel LEDs and issue diagnostic console messages.

A block diagram of the reset connections on the IMS B103 is shown in figure 1.2.

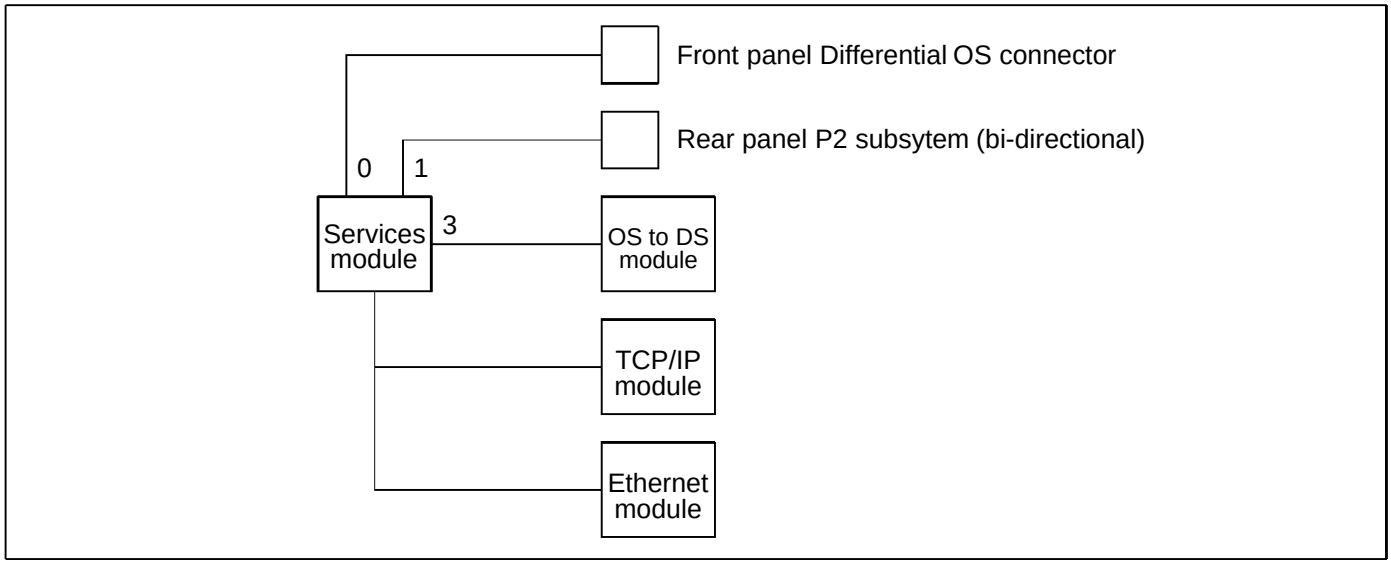

Figure 1.2 IMS B103 reset connections

The board as a whole is reset from one of the following sources:

- *SYSRESET on the P1 connector
- Front panel differential OS connector
- Power on reset
- Rear P2 subsystem if the direction is set to Up, (ie jumper J3 not present)

The TCP/IP and Ethernet modules are reset at the same time as the board. The subsystem ports 0, 1 and 3 pass through the board reset such that when the board is reset, all attached subsystems are also reset.

1.2.1 TCP/IP specification

Protocols

The TCP/IP Internet Protocol Suite, often referred to as just TCP/IP, was developed for the DARPA/ NSF Internet, now connecting a vast number of academic institutions and businesses worldwide. The TCP/IP protocols have proved so popular that they are also used for many networks not connected to the Internet.

The IMS B103 incorporates the IMS F103 TCP/IP firmware, implementing the following protocol elements:

- Ethernet Data Link Layer – Ethernet packetisation of IP layer datagrams is as specified in Internet standard RFC894 (i.e. Ethernet V2 Packetisation).
- ARP Address Resolution Protocol – the dynamic resolution of Ethernet addresses is designed to meet Internet standards RFC 826 and RFC1122.
- ICMP control protocol – connectionless information and error transfer between machines and gateways designed to meet RFC792 and RFC 1122.
- IP network layer – designed to meet Internet standards RFC791 and RFC1122 for IP layer behavior.
- TCP and UDP transport services – The TCP implementation provides a reliable, connection oriented transport layer, designed to meet Internet standards RFC793 and RFC1122. UDP provides a datagram service, implemented to RFC768 and RFC1122.
- SNMP management agent – The implementation is designed to meet Internet standards described in RFC1155, RFC1156 and RFC1157.
- TFTP file transfer – to meet RFC1350.
- BOOTP boot protocol – to meet RFC951.

Autonomous network booting

Using its ROM based TCP/IP implementation the IMS B103 can offer semi-automatic bootstrap of its OS to DS conversion transputer subsystem. This is performed from server resident binary files using the TFTP network service. The facility is equivalent to the bootstrap of diskless workstations. The application loaded into this transputer (or any network of IMS T4xx/T8xx transputers associated with this subsystem) can use any combination of network facilities to support its operation via run time libraries which access the TCP/IP stack across the bootstrap link.

Network performance

Support for standardised socket-based communication is provided for application code running on the OS to DS module via a series of run-time libraries. Network data rates of over 300kBytes/s can be achieved from this interface, with higher level protocols, such as NFS, being built on top of the basic socket protocols.

A primary use for these facilities is to provide a network based T9000 development interface service.

1.2.2 Software environment and configuration

Network Management

The IMS B103 incorporates Simple Network Management Protocol (SNMP) facilities compatible with standardised network management products used for the rest of your equipment. SNMP based facilities include standard statistics and integrity monitoring alongside IMS B103 specific functions.

Configuration

In order to minimise the configuration requirements of the IMS B103, the network implementation can utilise the BOOTP and TFTP protocols to determine network and bootstrap parameters. For this operation to succeed, it is necessary to have BOOTP and TFTP servers elsewhere in the network.

Both network configuration and bootstrap functionality can additionally be setup using an ASCII terminal attached to the IMS B103 serial port. This can be used for confirmation of correct operation or when TFTP and BOOTP services do not exist in the local network. Full SNMP functionality does, however, require file based configuration.

1.3 IMS B103 configuration

1.3.1 DS-Link interfaces

The OS to DS conversion module provides a flexible environment which supports IMS T9000 and DS-Link based applications or development environments. An IMS T805 transputer is combined with 4MB of DRAM and 4 STC101 DS-Link peripheral devices to provide two complete DS-Link based control development interfaces. One of these sets of signals is routed to the rear VME P2 connector whilst the other is available through differentially buffered DS-Link modular connectors on the front panel.

OS to DS conversion module memory map

The OS to DS conversion module memory map is as follows:

Description	Start	End
DRAM	#80001000	#803FFFFF
C101 rear **Reset**	#00000000	
C101 front **Reset**	#00001000	
C101 rear **Data** registers	#00004000	#00004FFF
C101 rear **Control** registers	#00005000	#00005FFF
C101 front **Data** registers	#00006000	#00006FFF
C101 front **Control** registers	#00007000	#00007FFF

Table 1.1 IMS T805 memory

The **Reset** registers are read/write registers. Data bit 0 is used to assert or de-assert the external reset line on a write, and confirmation is achieved by reading back from the same location. For the front panel external reset, when the register is read, the value represents the state of the reset return signal in the reset connector, (**notResetAck**). With the back panel external reset (**notDSRESET**) the value represents the state of the reset out line on the P2 connector. Each reset line resets both its associated IMS C101 and target T9000 network.

For the STC101 registers, address bits **MemA(5..0)** are ignored such that a block of 32 bytes can be block moved to a single register within the STC101, (useful for filling/emptying the STC101 FIFO using block write/read operations). Therefore, register addresses within the STC101 are arranged from 0, 1, 2 etc. On the IMS B103 they are 0, 32, 64, 96 etc.

All interrupt lines from the STC101 devices are ORed into the **Event** pin of the IMS T805 on this module. For further details of the STC101 refer to [5].

1.3.2 Jumpers and jumper settings

The overall layout of the IMS B103 and jumper positions is shown in figure 1.3. The following jumper descriptions demonstrate the full range of configuration options for the IMS B103 hardware. The IMS B103 as supplied, is configured with a default subset of these jumper settings that is compatible with the uses of the pre-programmed firmware.

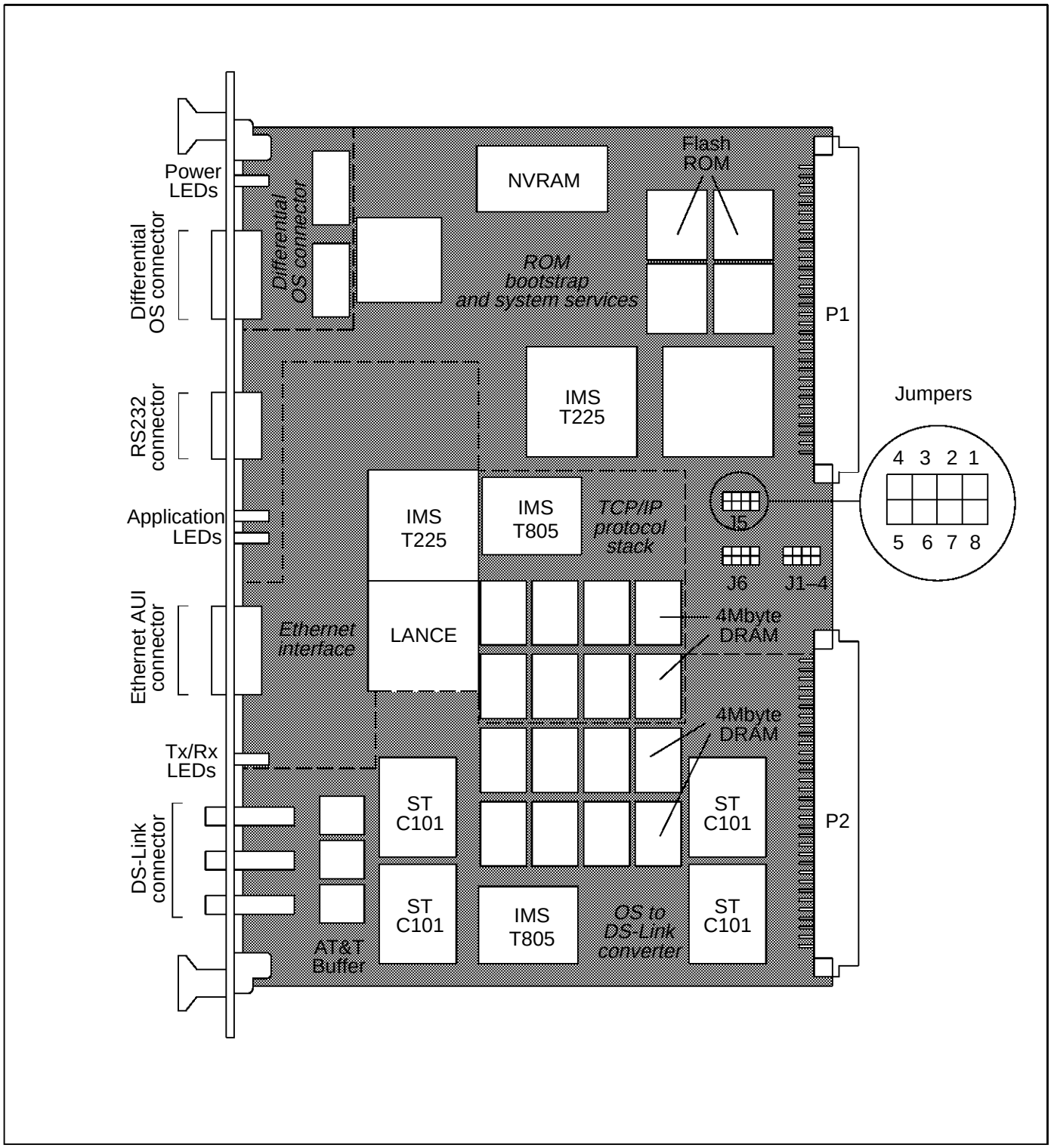

Figure 1.3 Board layout

1.3.3 Jumpers J1 to J4

Jumper	Present	Not present	Notes
1	Link Speed = 10Mb/s	Link speed = 20Mb/s	1
2	Link Speed = 10Mb/s	Link speed = 20Mb/s	2
3	P2 OS SubsystemDown	P2 OS SubsystemUp	
4	Boot from link	Boot from ROM	

Notes

1 For all links except OS to DS module Link0

2 Only for OS to DS module Link0

Table 1.2 Jumpers J1 to J4 designations

1.3.4 Jumpers J5 and J6

Jumper pin block number	Function
1	OS to DS (Link0)
2	Ethernet (Link1)
3	OS to DS (Link2)
4	OS to DS (Link3)
5	TCP/IP (Link0)
6	BACK
7	Services (Link3)
8	FRONT

Table 1.3 Jumper pin block designation for J5 and J6

1.3.5 Default configuration

The arrangement of links in figure 1.4 is the default configuration for the IMS B103 board and pre-programmed TCP/IP firmware.

1.3.6 Alternative configurations

Figures 1.5 and 1.6 demonstrate alternative configurations of the IMS B103 modules available through the user-selectable jumper blocks.
Note: The software support for these alternative configurations may require specific development.

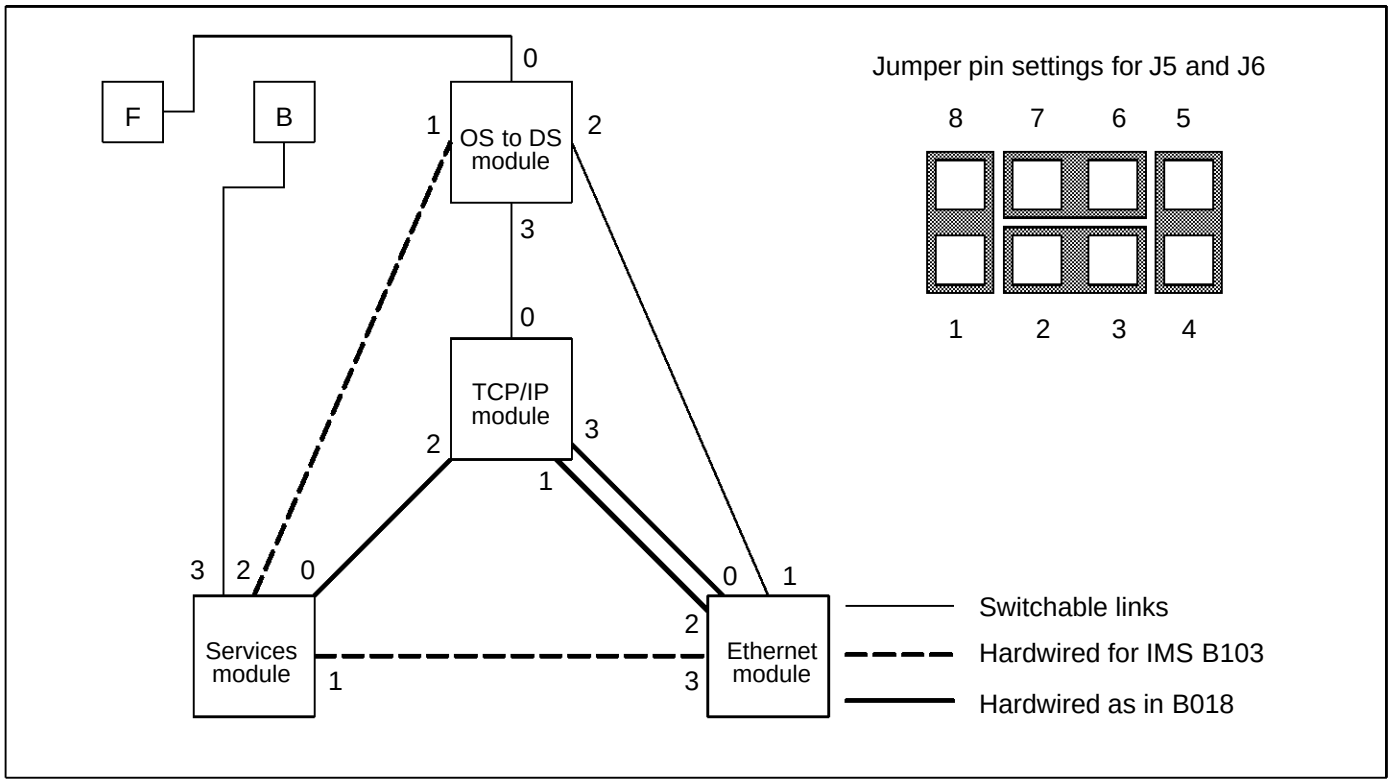

Figure 1.4 System 9000 module configuration

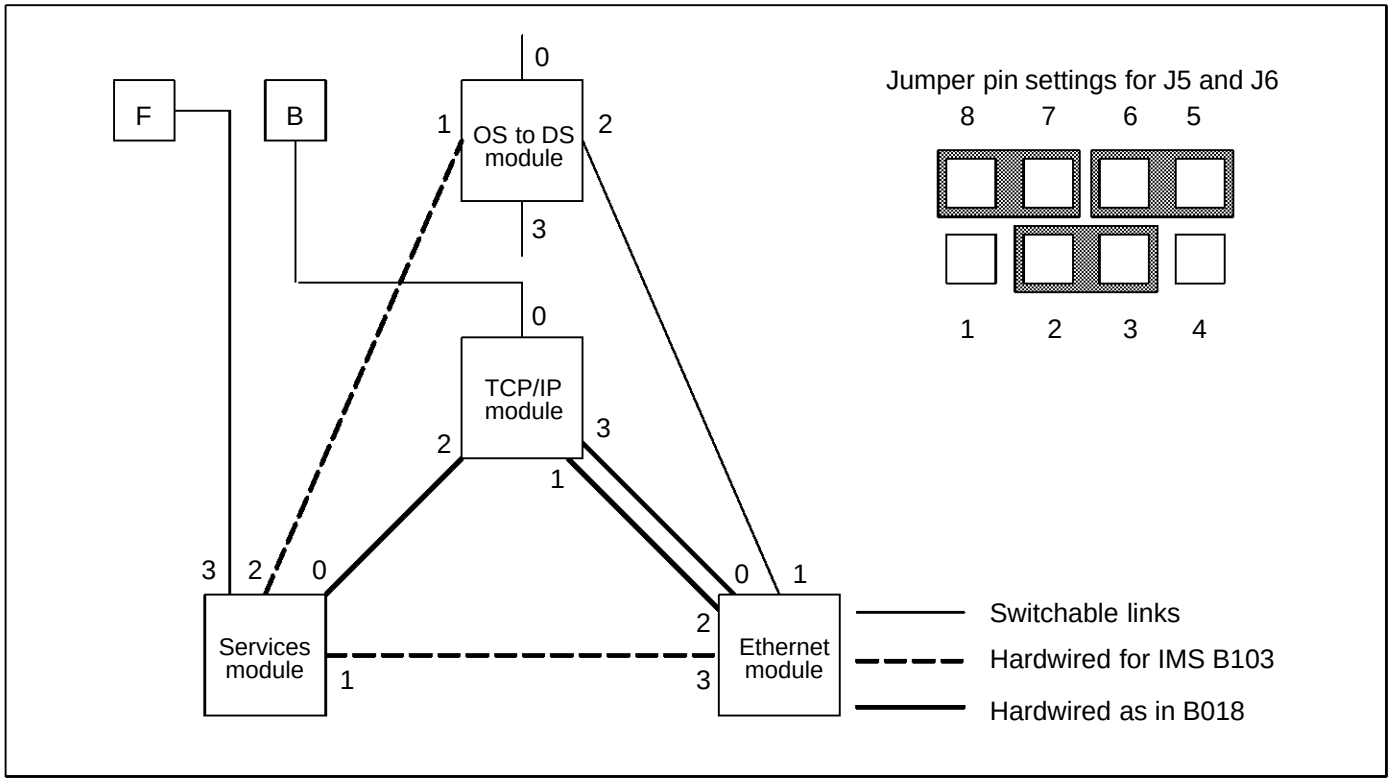

Figure 1.5 IMS B300-like module configuration

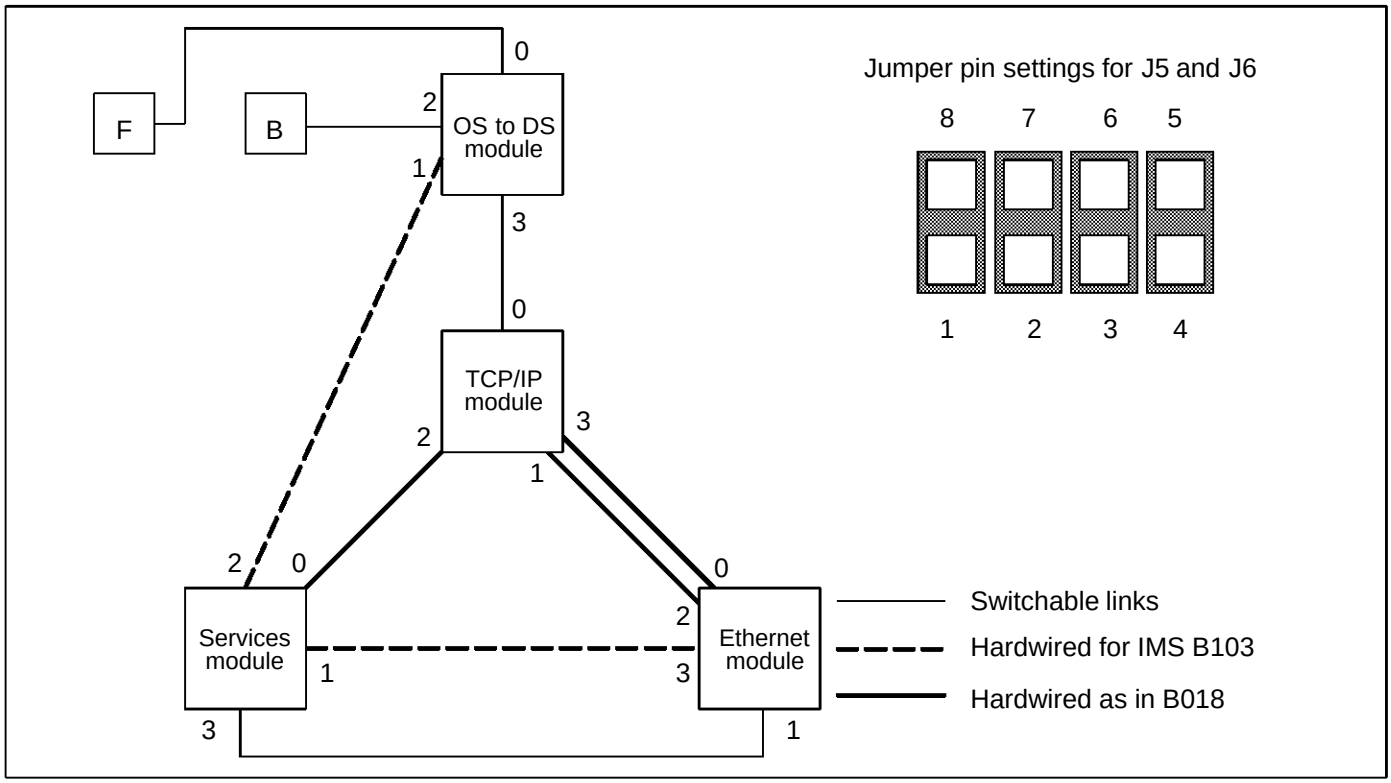

Figure 1.6 IMS F103-B300 network configuration

1.4 Front and back panel connections

The layout of the IMS B103 front panel is shown in figure 1.7. The following sections describe the function of the various connections and features.

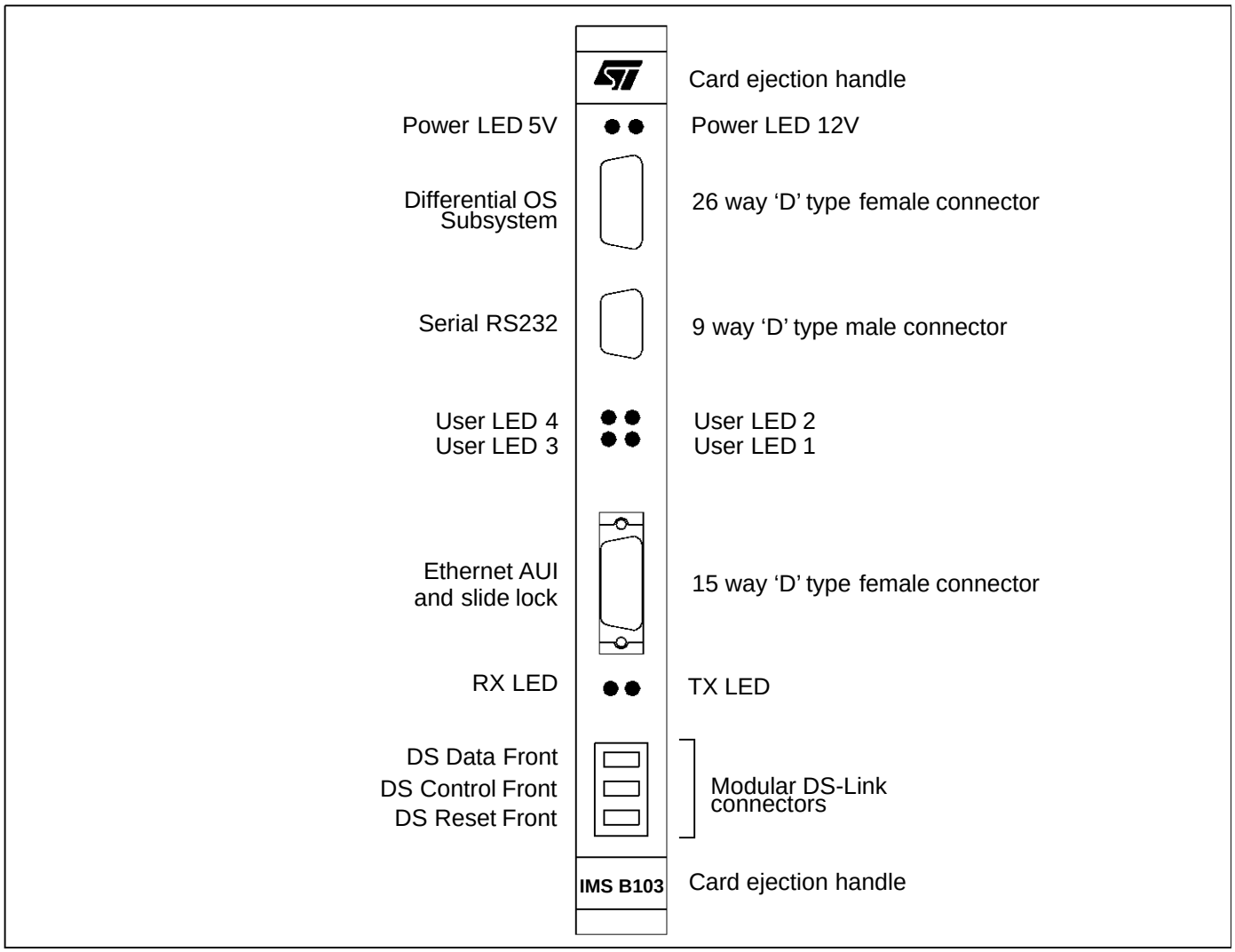

Figure 1.7 Front panel connections

1.4.1 LEDs

Two LEDs near the top of the panel are used to display the status of the +5V and +12V lines to the board. Both power rails must be present for satisfactory operation. Two additional LEDs, near the bottom part of the panel are used by the TCP/IP firmware to indicate transmission/reception of Ethernet packets – a useful indication of successful network connection.

Four user defined LEDs are also provided. These can be manipulated by software running on the OS to DS module.

1.4.2 OS link interfaces

A differentially driven OS link and subsystem port is provided on the front panel. The 26 way female ‘D’ type connector is wired as shown in figure 1.8, and is compatible with the IMS B300, IMS B019 and IMS CA15/16 products.

This connector can be used as an output or an input to the system. Suitable application software to support its operation must be used in either case.

A single ended OS link and subsytem port is provided on the VME P2 connector. Depending on the jumper configuration this can be configured in various different ways to suit specific applications. The pinouts of this P2 connection are compatible with standard INMOS link and subsystem jumper cables.

The front panel OS link subsystem connector provides both an Up and Down subsystem connection. The rear P2 OS link subsystem provides either an Up or Down subsystem via jumper J3.

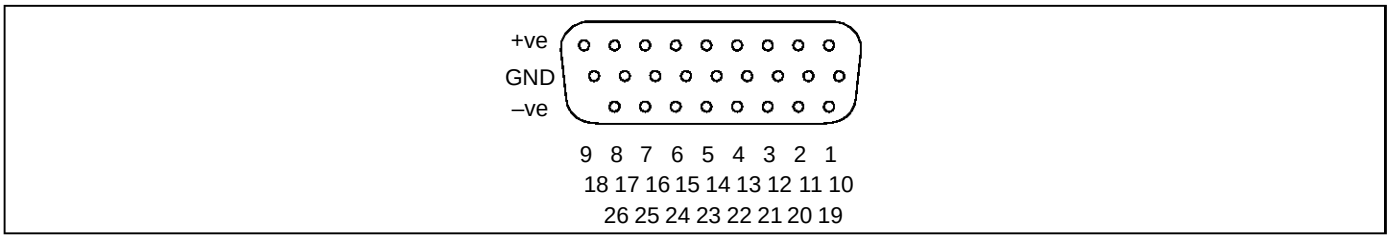

Figure 1.8 Differential OS connector (viewed from front panel)

Pin	Signal	Pin	Signal
1	SubSystemDownReset+	14	Ground
2	SubSystemDownAnalyse+	15	Ground
3	SubSystemDownError+	16	Ground
4	SubSystemUpReset+	17	Ground
5	SubSystemUpAnalyse+	18	Ground
6	SubSystemUpError+	19	SubSystemDownReset–
7	LinkOut+	20	SubSystemDownAnalyse–
8	LinkIn+	21	SubSystemDownError–
9	Ground	22	SubSystemUpReset–
10	Ground	23	SubSystemUpAnalyse–
11	Ground	24	SubSystemUpError–
12	Ground	25	LinkOut–
13	Ground	26	LinkIn–

Table 1.4 Subsystem link connector pinout

1.4.3 DS-Link interfaces

Both front and back panel DS-Link connections are provided on the IMS B103 to support the primary use of the board as a network interface to a T9000 development system. The front panel connectors are differentially driven and are presented as standard modular DS-Link connectors. A differential hardware reset signal is provided along with control and data link connections.

Via the P2 VME connector an independent set of similar single ended signals are provided to support close coupling of the IMS B103 interface and T9000 target hardware within the same enclosure. The pin assignment for the P2 connector is given in figure 1.9.

	C	B	A	
1		VCC		
2		GND		
3				
4				
5				
6				
7				
8				
9				
10				
11				
12		GND		
13		VCC		
14				
15				
16				
17				
18				
19	DIN			Data rear
20	GND			
21	SIN			
22	SOUT	GND		
23	GND		GND	
24	DOUT		N/C	
25	DIN		OSLINKOUT	OS-Link rear
26	SIN		OSLINKIN	
27	GND		GND	
28	SOUT		notOSRESET	Control rear
29	DOUT		notOSANALYSE	
30	notDSRESET		notOSERROR	OS subsystem rear
31	VCC	GND	VCC	
32	VCC	VCC	VCC	

Figure 1.9 P2 connector pinout

1.4.4 Diagnostic and configuration terminal

A 9 way male ‘D’ type connector, conforming to PC conventions is provided to connect an RS232-based serial console to the IMS B103 for configuration and display of diagnostic messages. The pinout of this connector is given in figure 1.10 and table 1.5.

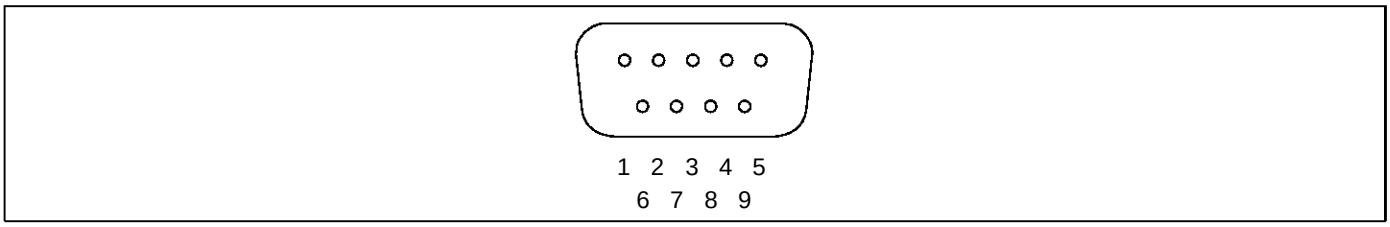

Figure 1.10 Serial connector (viewed from front panel)

Pin	Signal	Pin	Signal
1	N/C	6	N/C
2	Rx data	7	RTS
3	Tx data	8	N/C
4	DTR	9	N/C
5	Ground		

Table 1.5 Serial connector pinout

1.4.5 Ethernet AUI

A standard Ethernet AUI connection is provided on the front panel of the IMS B103. The pinout for this connection is given in figure 1.11 and table 1.6.

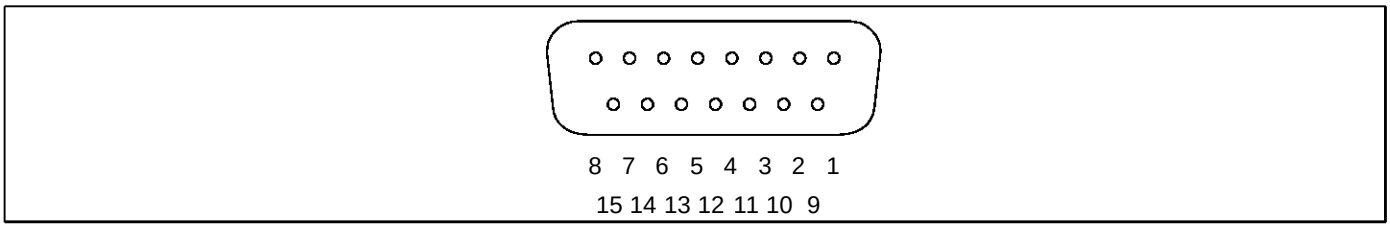

Figure 1.11 Ethernet connector (viewed from front panel)

Pin	Signal	Pin	Signal
1	Logic Ref	9	Collision–
2	Collision+	10	Transmit–
3	Transmit+	11	Logic Ref
4	Logic Ref	12	Receive–
5	Receive+	13	Power
6	Power return	14	Logic Ref
7	N/C	15	N/C
8	Logic Ref		

Table 1.6 Ethernet connector pinout

1.4.6 VME interface

The P1 connector of the VMEbus is used for only a small subset of its signals, its principle use being to supply power to the IMS B103. The pin assignment of the P1 connector is given in figure 1.12.

Pin	Row C	Row B	Row A
1			
2			
3			
4		***BG0IN**	
5		***BG0OUT**	
6		***BG1IN**	
7		***BG1OUT**	
8		***BG2IN**	
9	**GND**	***BG2OUT**	**GND**
10		***BG3IN**	
11		***BG3OUT**	**GND**
12	***SYSRESET**		
13			
14			
15			**GND**
16			
17			**GND**
18			
19			**GND**
20		**GND**	
21			*** IACKIN**
22			***IACKOUT**
23		**GND**	
24			
25			
26			
27			
28			
29			
30			
31	**+12V**		**–12V**
32	**+5V**	**+5V**	**+5V**

Note: All remaining pins are not connected

Figure 1.12 P1 connections

1.5 Firmware configuration

The IMS B103 is supplied with pre-programmed TCP/IP firmware that enables the board to be used within a development or application system environment with the minimum of configuration. The required configuration operations are performed via the serial diagnostic console and/or via files located on a centralized network server machine. At any time, via an attached serial console, a simple interactive display can be used to display operational statistics or edit the configuration variables. The values are preserved through power cycles by storage in an area of non volatile RAM.

The configuration data required is summarised below.

- Ethernet Address: Permanently programmed into the firmware at time of manufacture
- IP address: Internet address assigned to this node in the user's local network
- System Name: The name of the node associated with the IP address
- Domain: The internet domain in which the system is located
- Subnet mask: Significant bits of the IP address for local domain
- Broadcast address Significant bits of the IP address for localised network broadcasts
- Name Server 1: IP address of a local node which is running the IP name resolution protocol server (or 0.0.0.0 if none)
- Name Server 2: IP address of an alternate local node which is running the IP name resolution protocol server (or 0.0.0.0)
- TFTP server 1: IP address of a local node which is running the IP Trivial File Transfer Protocol (TFTP) service.
- TFTP server 2: IP address of an alternate local node which is running the IP Trivial File Transfer Protocol (TFTP) service.
- Boot File: Name of transputer executable file that will be loaded at boot time into the OS to DS subsystem module
- Network Config: T or F to enable or disable use of TFTP server to obtain self configuration data.

The IMS B103 uses the address of the TFTP server machines to locate and read both self configuration files (which are given names derived from the IP address of the node with a .CNF suffix) and the executable code that will be loaded after initialization onto the OS to DS conversion module or any other transputer network that is connected to this subsystem.

1.6 Example application

A principle application for the IMS B103 is as the heart of an Ethernet based IMS T9000 development system. In the configuration illustrated in figure 1.13, the IMS B103 boots IMS T9000 Network Control Software onto its OS/DS conversion subsystem which then offers a socket based connection to hosted development tools, (Sun or PC based). The DS-Link signals from the IMS B103 are connected to an HTRAM network formed from a VME motherboard (IMS B101) and housed in an IMS B150 development rack.

Any user wishing to access the IMS T9000 system runs a host server which connects to the IMS B103 based Network Control Software and offers bootstrap, control and application services to the code running on the HTRAM devices.

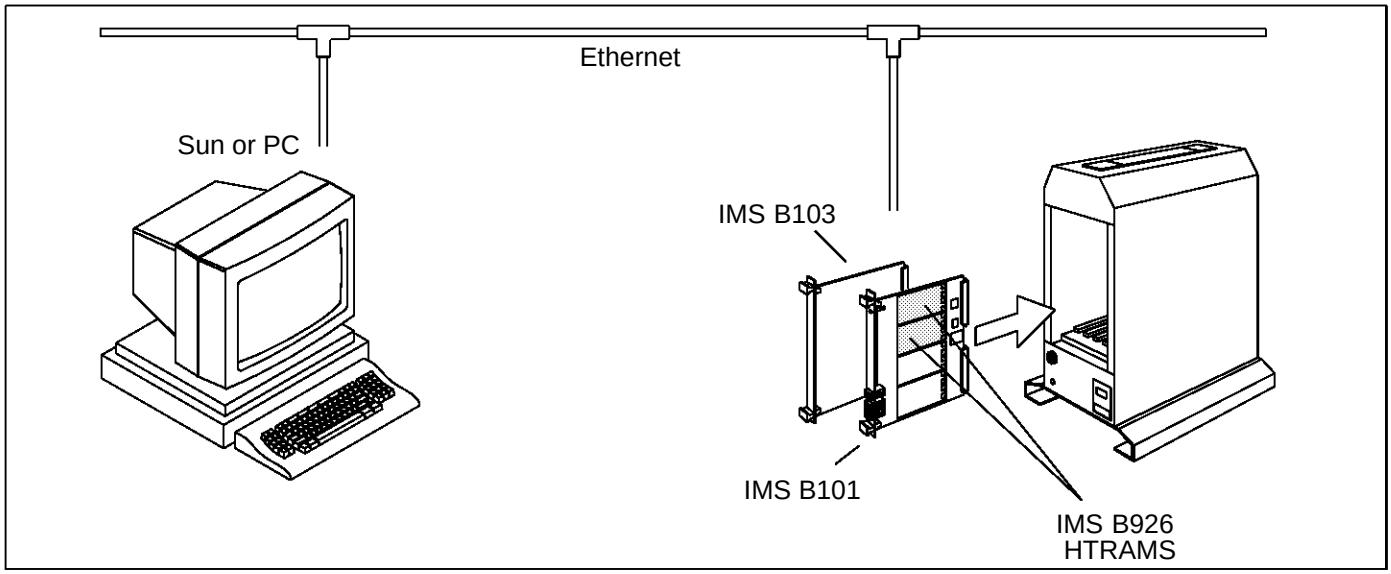

Figure 1.13 Example application

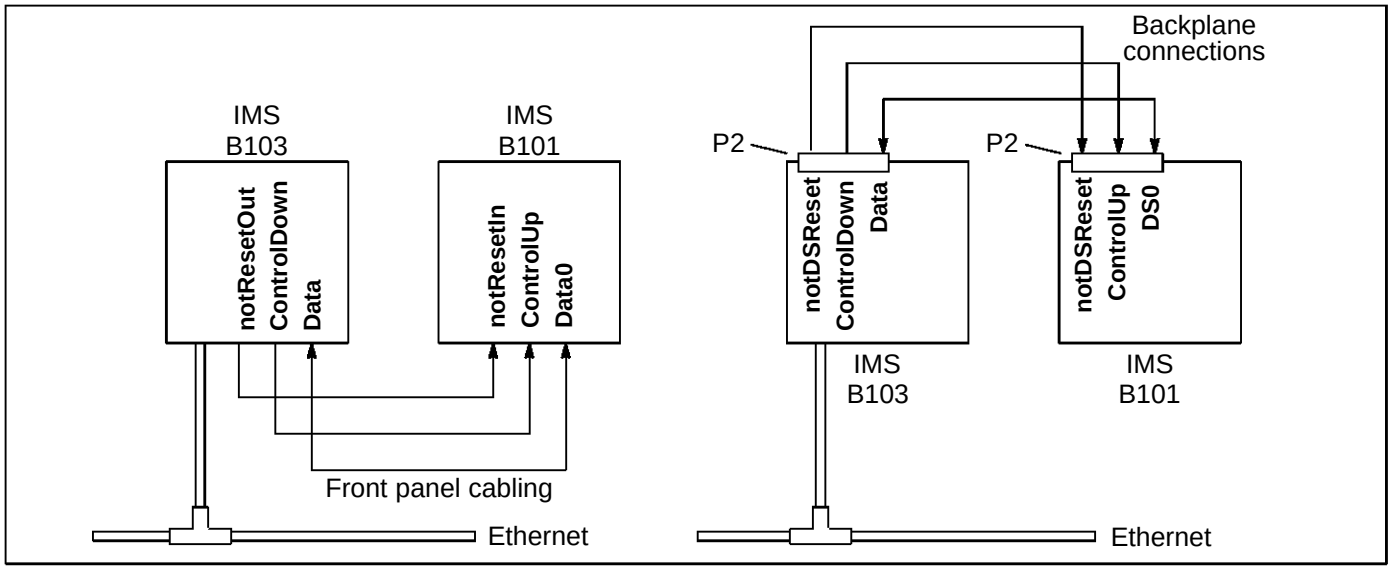

Figure 1.14 Connections between an IMS B101 and IMS B103

1.7 Electrical specification

The IMS B103 requires a +5V power supply in accordance with the VMEbus specification. That is, the +5V DC supply must be between 4.75V and 5.25V and have less than 50mV pk-pk noise and ripple between DC and 10MHz. A +12V power supply in accordance with the VMEBus specification is also required to power an Ethernet transceiver. The IMS B103 does not incorporate protection against incorrect power supplies. Major damage can result from operating the board outside its power supply range.

1.7.1 Environmental details

Parameter	Operating	Storage
Temperature	0 to 50°C ambient air	–55 to 85°C
Relative humidity	95% non condensing	95% non condensing
Thermal shock	< 0.08°C/s	< 0.15°C/s
Altitude	–300 to +3000m	–300 to +16000m

Table 1.7 Environmental Details

1.8 Field support

INMOS products are supported worldwide through SGS-THOMSON Sales Offices, Regional Technology Centres, and authorised distributors.

1.9 Ordering information

Description	Order number
IMS B103 Ethernet to DS interface	IMS B103-1

1.10 References

1 *T9000 Transputer Hardware Reference Manual*, INMOS Ltd 1993.

2 *The VMEbus Specification rev C.1*, Motorola, 1985.

3 *HTRAM Specification*, INMOS Ltd 1994.

4 *IMS B300 datasheet*, INMOS Ltd 1994, (42 1493 02).

5 *STC101 datasheet*, INMOS Ltd 1993

6 *IEEE Standard for a Versatile Backplane Bus: VMEbus*, IEEE 1987.

7 *The Transputer Development and iq systems Databook*, INMOS Ltd (72 TRN 219 01).